**Application No.: 10/783,025**

AMENDMENT TO SPECIFICATION

**Please amend the paragraph on page 11, beginning at line 9 as follows:**

Each of the connection switching circuits **131** through **13n** includes: a level shifter **LS** for receiving a voltage input from the input terminal [[**VI**]] **VIN** and an associated one of the boosting ability switching signals **EN1** through **ENn**; and first and second p-transistors **Mc1** and **Mc2** which are connected to the respective opposed electrodes of the boosting capacitor **CP** in series and have their gates connected to an output terminal of the level shifter **LS**.

**Please amend the paragraph on page 15, beginning at line 11 as follows:**

Each of the clock amplitude switching circuits **51** and **52** provided between the boosting section **10A** and the boosting clock control circuit **140** includes: a p-transistor **M24** having its source connected to a power supply voltage VDD; and a fourth n-transistor **M25** having its source connected to a ground voltage VSS. Between the drains of the p-transistor **M24** and the [[four]] fourth n-transistor **M25**, n n-transistors **MNv1** through **MNvn** (where n is an integer of one or more) each of which has its gate and drain are connected to each other and is used for switching the amplitude of the input clock signal CLK1 or CLK2 are connected in series. The gates of the p-transistor **M24** and the fourth n-transistor **M25** are connected to each other, and the clock signal CLK1 or the clock signal CLK2, which is complementary to the clock signal CLK1, is input to this common gate. In addition, n p-transistors **MPv1** through **MPvn** as switching elements are connected to the drains and sources of the respective associated n-transistors **MNv1** through **MNvn**. The boosting ability control signals EN1 through ENn are input to the respective gates of the p-transistors **MPv1** through **MPvn**.

**Application No.: 10/783,025**

**Please amend the paragraph on page 22, beginning at line 11 as follows:**

Each of the boosting cells **41** through **43** includes: three charge transfer n-transistors **M41** through **M43** provided between an input terminal **VIN** and an output terminal **VO** and connected in parallel; gate boosting capacitors **Cg1** through **Cg3** connected to the gates of the respective charge transfer transistors **M41** through **M43** and driving the gates; three switching transistors **SW1** through **SW3** connected in series between the gates and drains of the respective charge transfer transistors **M41** through **M43** and serving as n-transistors for establishing electrical connections or disconnections between the gates and the drains; and a boosting capacitor **CP** provided between the output terminal **VO** and a boosting clock input terminal **CLKM** to which the clock signal CLK1 or CLK2 is input. In this embodiment, the three charge transfer transistors ~~41 through 43~~ M41 through M43 are provided. However, the number of charge transfer transistors is not limited to this specific embodiment.